AMENDMENTS TO THE SPECIFICATION

I. Please replace the Abstract with the following amended Abstract:

A circuit structure and signal encoding method for a serial ATA external physical layer is provided. The circuit structure and signal encoding method thereof is capable of reducing the number of interface signals of a serial ATA external physical layer, essentially comprising a decoder/encoder, a serializer/deserializer, a phase locked loop, at least one transmitter ~~transmitters~~, at least one receiver ~~receivers~~, and at least one OOB signal detector ~~detectors~~, encoding various control signals and various status signals, required for the connection between the decoder/encoder and a storage medium controller, into data signals using signals other than a data conversion requirement of 8bits and 10bits, by the ~~means of a~~ decoder/encoder, in order for greatly reducing the number of interface signals required for the connection between the external physical layer and a main control chip.

II. Please replace the paragraph, Page 1, Line 9 to Line 20 with the following amended paragraph:

In these days, as the high development in the information related industry and the need for information products with high operation and transmission speed increasingly, the industries may be forced to devote themselves in developing various transmission interface requirements. In terms of the storage interface, from the ATA (Advanced Technology Attachment) interface with a transmission rate of 16MBps in the early phase, through the ATA33 interface with a

transmission rate of 33MBps, and the ATA66 interface with a transmission rate of 66MBps, until the ATA100 ~~ATA-100~~ and ATA133 interface requirements, etc., all of them are confined by parallel data transmission, such that the amount of the signal lines used for transmission, the noise interference, the limitation on the length of the transmission lines, and the difficulty for raising the transmission rate are greater in the aforementioned interface requirements.

III. Please replace the paragraph, Page 2, Line 3 to Line 8 with the following amended paragraph:

Another solution proposed by the industry is shown in Fig. 1, wherein a part of circuit in the serial ATA physical layer is made independently in a serial ATA external physical layer 161. A storage medium controller 121 in a main control chip 12 may be connected to a serial ATA device 16 (a serial ATA hard disk, for instance) via the serial ATA external physical layer 161, other than connected to a parallel ATA device 18 (a parallel ATA hard disk, for example) via an IDE bus 14(Integrated Drive Electronics) .

IV. Please replace the paragraph, Page 3, Line 7 to Line 33 with the following amended paragraph:

For the purpose of achieving aforementioned objects, the present invention provides a circuit structure for a serial ATA external physical layer, essentially comprising a decoder/encoder connected to a storage medium controller via a set of parallel signal

transmission lines and a set of parallel signal receiving lines for decoding a parallel transmission signal originated from the storage medium controller into a parallel transmission data signal and at least one control signals; a serializer/deserializer connected to the decoder/encoder for the conversion of the parallel transmission data signal into a serial transmission data signal; a phase locked loop connected to the decoder/encoder and the serializer/deserializer, respectively, for receiving the control signals originated form the decoder/encoder, as well as generating clock signals required for the operation of the physical layer and transmitting a reference clock signal to the storage medium controller; at least one transmitters, connected to the serializer/deserializer, each of the transmitters being used to transmit the serial transmission data signal to a serial ATA device connected thereto via a set of serial signal transmission lines; at least one receivers connected to the serializer/deserializer, each of the receivers being used to transmit a serial receiving data signal received from the serial ATA device connected thereto to the serializer/deserializer, and then the serial receiving data signal being converted into a parallel receiving data signal by the serializer/deserializer for transmitting to the decoder/encoder; and at least one out of band (OOB) signal detectors connected to receiving signal lines of the corresponding receivers, respectively, for detecting the operation condition of the serial ATA device and transmitting at least one sets of detected status signals to the decoder/encoder, the parallel receiving data signal and the status signals then being encoded into a parallel receiving signal by the decoder/encoder and, afterward, transmitted to the storage medium controller via the set of parallel signal receiving lines, in order for reducing the number of interface signals required for transmission.